Remarks/Arguments

Examiner Paul Kim is thanked for the thorough Office Action.

In the Claims

Claim 1, step a is amended as follows "obtaining test measurement values on a device ~~at a plurality~~ of one or more ~~of~~ independent variable values; " This amendment corrects and clarifies that "test measurement values" from one or more independent variables are need to perform the method. For support see spec. p. 11, lines 17 to 20. See the example of one independent variable. See especially, spec. p. 13, L-15-18. See generally, Spec. p. 12, L 16, to P. 14, Line 14. Also, See spec. 15, lines 21 and 22.

Another example on one independent variable is in figure 5A where 1/Temperature is the one independent variable and resistance is the dependent variable.

No new matter is added.

This is not an amendment made in response to prior art and should not invoke FESTO limitations.

35 USC 102 Rejections

Rejection of Claims 1 and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsushita.

The rejection of Claims 1 and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsushita is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the following remarks.

1. (CURRENTLY AMENDED) A test method comprising:
   a) obtaining test measurement values on a device ~~at a plurality~~ of one or more ~~of~~ independent variable values;
   b) calculating the goodness of fit value for a fitted curve between :
      (1) said test measurement values; and
      (2) the independent variable values;
using said goodness of fit value to monitor the processes used to form said device.

The instant office action posits:

> With regard to claims 1, 5, and 6, Matsushita teaches a test method comprising: obtaining test measurement values on a device at a plurality of independent variable values (col. 2, lines 10-22), calculating goodness of fit value for a fitted curve between a resistance and independent value (fig. 2), and using the goodness of fit to monitor the process (col. 1, lines 28-33).
> With regard to claim 4, Matsushita teaches the goodness of fit being a standard error measurement (col. 1, lines 60-62).

Table 1 below summarizes some of the differences between claim 1 and Matsushita.

Table 1:

Claim 1	Matsushita
1.(CURRENLTY AMENDED) A test method comprising:	
a) obtaining test measurement values on a device ~~at a plurality~~ of one or more ~~of~~ independent variable values;	
b) calculating the goodness of fit value for a fitted curve between : (1) said test measurement values; and (2) the independent variable values;	Different – See figure 2 – Teaches against claim 1(step b) by teaching only one (not more than one) independent variable value. – Teaches only thickness
c) using said goodness of fit value to monitor the processes used to form said device.	different – see (col. 1, lines 28-33).- no suggestion of claim 1 step (c) – see Therefore, it is necessary to measure the thickness of an insulating layer which has been formed on wiring patterns and flattened by using planarization(flattering) technique, for example, when designing semiconductor device manufacturing process so as to know the uneven step coverage of a base.

As shown above in table 1, Matsushito teaches against applicant's claim 1. For example, Matsushito does not suggest claim 1 step c; "c) using said goodness of fit value to monitor the processes used to form said device."

The spec, p. 14, line9 to 11 and figure 4B shows an example of claim 1, step c) .

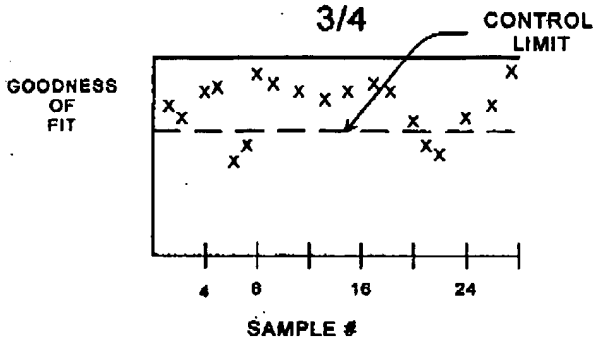


FIGURE 4B

In contrast, Matshuhito teaches against claim 1,step (c) by using the thickness measurement to control the line. Matshuhito controls by the correlation curve, not by claim 1's "goodness of fit value". Moreover, applicant could not find any discussion in Matshuhito related to "goodness of fit tests. See col. 7 L 59 t o co. 8, L 28. Furthermore, the office action cites Matshuhito fig 2 as support for a "goodness of fit test". However, figure 2 merely shows a plot of resistance vs. Thickness, not a "goodness of fit test".

For these reasons, claim 1 is not anticipated by Matshuhito and is obvious over Matshuhito.

Claim 4 is non-obvious over Matsushita US 6,218,847

Claim 4 states:

(ORIGINAL) The method of claim 1 wherein the goodness of fit is a correlation coefficient or a standard error measurement.

The office action posits that "With regard to claim 4, Matsushita teaches the goodness of fit being a standard error measurement (col. 1, lines 60-62).:

Matsushita (col. 1, lines 60-62).: states:

On the other hand, if the thickness of an insulating film on fine wiring patterns where the surface area of a wiring member (a conductive layer) forming wiring patterns are small or the width of the wiring member (conductive layer) is narrow, then a measurement error becomes large and the film thickness cannot be measured at high precision.

Applicant respectfully submits that Matsushita US 6,218,847 does not suggest applicant's claim 4 because Matsushita merely states that it is hard to measure thin film thicknesses, not claim 4 limitations.

Claims 5-6 are non-obvious

Claims 5 and 6 are non-obvious because they depend from non-obvious claim 1 for the reasons stated above.

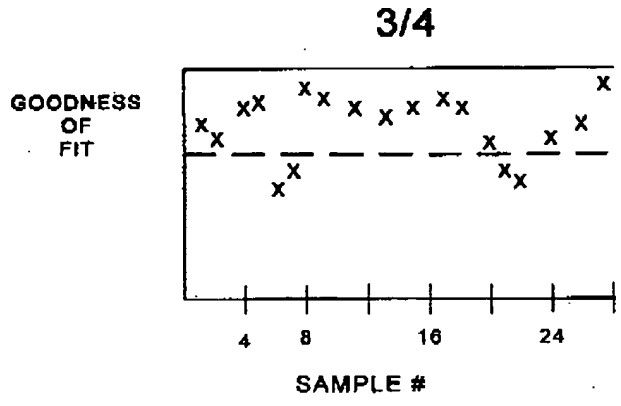
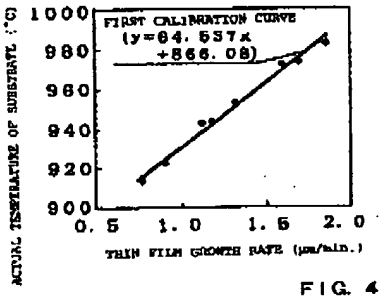
Rejection of Claims 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kashino et al.

The rejection of Claims 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kashino et al. is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

The instant office action argues that :

> With regard to claim 25, Kashino et al teaches providing a device structure that has a first test structure in which a test measurement can be obtained (col. 2, lines 1), measuring a first test measurement (col. 5, lines 20), calculating a goodness of fit value for a fitted curve between a first and second test measurement under a first and second test condition (fig. 2), and using the goodness of fit value to control the processes used to form the test structure (col. 2, lines 39-42).

Kashino does not meet or suggest claim 25, step (d). " using said goodness of fit measurement to: (1) control the processes used to form the device or (2) screen the devices." Kashino (col. 2, lines 39-42) does not even appear to mention any goodness of fit measurement (such as correlation coefficient, ect.). Kashino figure 1 and the entire patent do not mention goodness of fit tests nor does it suggest the "goodness of fit " measurement (e.g., correlation coefficient) can be use to control or screen the devices.

applicant example of claim 26, step d)	Kashino
 FIGURE 4B	 FIG. 4

Kashino (abstract, claims, summary of invention) shows method to perform several correlations. Kashino does not suggest claim 26, step (d).

Claim 26 Is Non-Obvious Over Kashino

The instant Office action argues that:

> **With regard to claim 26,. Kashino et al teaches the first and second test conditions being different temperatures (fig. 1, step S2).**

As discussed above kashino does not suggest parent claim 26. Therefore, dependent claim 26 is non-obvious.

CLAIM REJECTIONS - 35 USC § 103

Rejection of Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita in view of Littau et al.

The rejection of Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita in view of Littau et al. is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

The instant office action argues:

> Matsushita teaches goodness of fit being calculated does not specify control limits being used. Littau et al teaches control limits being used for determining goodness of fit parameters [107]. It would have been obvious to one of ordinary skill in the art at the time of the invention, to modify Matsushita, so that control limits are used, as taught by Littau et al, in order to improve legitimacy of calculated values.

Combination of reference is improper.

First, the combination of Matsushita and Liuttau is improper. The patents do not suggest combination, and do not solve a common or related problem. The patents teach against each other. This combination can only be done with hindsight.

Even if combined, the references do not suggest claims 2 and 3

Neither Matsushita and Liuttau or the combination of Matsushita and Liuttau suggests claim 1(c) using the ""goodness of fit test to monitor the process..." . The instant office action's cite of Luittau (para [107]) merely shows variation of a **direct measurement** of one parameter (e.g., CD) over time (not applicant's claims 1 and 2 and 3' a goodness of fit test).

For these reasons claims 2 and 3 are non-obvious.

Rejection of Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kashino et al in view of Park et al.

The rejection of Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kashino et al in view of Park et al. (para 7) is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the remarks.

Claim 21 states:

> 21. (ORIGINAL) A method for estimating defect levels by goodness of fit measurements related to resistance of an interconnect layer in a process for manufacturing an integrated circuit, said method comprising the steps of:
>
> a) fabricating on a wafer, using said manufacturing process at least a first test structure, a second test structure and a third type test structure incorporating a resistive portion from which a resistance is measured,
> b) said resistive portion having an effective length and an effective width, said effective length being substantially greater than said effective width and said effective width being selected to be substantially greater than an expected critical dimension loss for said process;
> c) measuring said resistance; and
> d) deriving the sheet resistance from the resistance measurement;
> e) calculating a goodness of fit value between the one divided by the sheet resistance (1/Rs) and a second parameter;
> f) using said goodness of fit value to: (1) control the processes used to form the test structures or (2) screen the test structures.

The instant office action argues:

> Kashino et al teaches a method comprising: fabricating multiple test structures on a wafer incorporating a resistive structure (col. 2, lines 1+), measuring the resistance and deriving the sheet resistance from the resistance measurement (col. 5, lines 20+),
> **calculating the goodness of fit value between one divided by the sheet resistance and a temperature (fig. 2)**, and using the goodness of fit value to control the processes used to form the test structure (col. 2, lines 39-42).
>
> Kashino et al, however, does not specify the resistive portion having an effective length and width, the effective length being substantially greater than the effective width.
> Park et al teaches a method for calculating goodness of fit of a wafer in which the effective length is substantially greater than the effective width (page 4, table 1). It would have been obvious to one of ordinary skill in the art at the time of the invention, to modify Kashino et al, so that the effective length is greater than the effective width, as taught by Park et al, in order to effectively monitor and control the fabrication process.

Claim 21	Kashino and Park et al.
21. (ORIGINAL) A method for estimating defect levels by goodness of fit measurements related to resistance of an interconnect layer in a process for manufacturing an integrated circuit, said method comprising the steps of:	
a) fabricating on a wafer, using said manufacturing process at least a first test structure, a second test structure and a third type test structure incorporating a resistive portion from which a resistance is measured,	
b) said resistive portion having an effective length and an effective width, said effective length being substantially greater than said effective width and said effective width being selected to be substantially greater than an expected critical dimension loss for said process;	different – park table 1 – teaches against-park table 1 shows a goodness of fit for a measurement for a spectrometer – See Park – [0047]
c) measuring said resistance; and	
d) deriving the sheet resistance from the resistance measurement;	

e) calculating a goodness of fit value between the one divided by the sheet resistance (1/Rs) and a second parameter;	Not Suggested by either reference – See Kashino col 2, LL 39-42.
f) using said goodness of fit value to: (1) control the processes used to form the test structures or (2) screen the test structures.	Not suggested -

As discussed previously above, Kashino does not suggest at least applicant's claim 21, steps e and f. Kashino merely makes calibration curves, but does not suggest applicant's monitoring a process using a "goodness of fit" value (e.g., correlation coefficient).

Improper combination of references.

The combination of Kashino and Park is improper.

The patents do not suggest combination, and do not solve a common or related problem. The patents teach against each other. Park is spectrometry thickness measurement unrelated to Kashino's temperature and implant calibrations. This combination can only be done with hindsight.

Park table 1 does not suggest claim 21.

Park table 1 is described in Park [0037] and [0051]. The goodness of fitness test in Park relates to some spectrometer measurement, (not claim 21' step (b) resistive structure or any other claim 21 steps.

Claim 22 is non-obvious

Claim 22 states

> 22. (ORIGINAL) The method of claim 21 where said second parameter is the effective width of the test structures or the temperature.

Neither Park nor Kashino suggest parent claim 21 or the limitations in claim 22.

Rejection of Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita in view of Park et al.

The rejection of Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita in view of Park et al. (para 8) is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

The instant office action in para 8 states:

> Matsushita teaches a test method comprising: providing a device structure for which a test parameter is measured (col. 2, lines 10-22), measuring the test values on the structure, calculating a good of fit value for a fitted curve between the resistance and dimensional measurement (fig. 2), and using the goodness of fit to control the process

The combination of reference is improper as discussed above.

Even if combined, the references do not suggest claim 23 limitations.

Table : Non-obvious difference between claim 23 and the references.

Claim 23	Matshushit and Park
23. (previously presented) A test method comprising:	
a) providing a device structure that has at least a first test structure, a second test structure and a third test structure from which a test parameter is measured;	not suggested – park teaches a goodness of fit test of a spectrometer , not the goodness of fit for a curve of claim 23, step (c) (1) and (2).
b) measuring the test parameter values on the test structures;	
c) calculating the goodness of fit value for a fitted curve between : (1) the test parameter values and (2) a dimensional measurement of the test structures;	**Not suggested**- neither reference suggest calculating the goodness of fit between the test parameter and the dimensional measurement.
d) using said goodness of fit value to: (1) control the processes used to form the device structures or (2) screen the device structures.	Not suggested. – no use of goodness of fit value to control or screen.

At least Claim 23, steps (a), (c) and (d) are not suggested as shown above in the table and discuss above in other rejections.

Allowable subject matter

The allowance of claims 7 to 20 is gratefully acknowledged.

All Pending Claims Addressed

It is believed that all the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not bee expressed. Finally, nothing in this paper should be construed as

an intent to concede any issue with regard to any claim, except as specifically stated in this paper. and the amendment of any claim does not necessarily signify concession of the unpatentability of the claim prior to its amendment.

CONCLUSION

In conclusion, reconsideration and withdrawal of the rejections are respectfully requested. Allowance of all claims is requested. Issuance of the application is requested.

It is requested that the Examiner telephone the undersigned attorney at (215) 670-2455 should there be anyway that we could help to place this Application in condition for Allowance.

Charge to Deposit Account

The Commissioner is hereby authorized to apply any fees or credits in this case, which are not already covered by check or credit card, to Deposit Account No. 502018 referencing this attorney docket. The Commissioner is also authorized to charge any additional fee under 37 CFR §1.16 and 1.17 to this Deposit Account.

Respectfully submitted,

Date: Oct 31, 2005

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